



Memory Population Guidelines for AMD EPYC™ 7002 Series Processors

Publication #	56502	Revision:	1.00
Issue Date:	August 2020		

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Revision History

Date	Revision	Description
August 2020	1.00	Initial Public release.

Introduction

The AMD EPYC™ 7002 Generation Processors are designed to build on the AMD EPYC 7001 processors' industry leading eight channels of DDR4 memory, bringing additional capabilities including significantly higher speed memory channels and a wider variety of DIMM types. Supported DIMM types include registered DIMMs (RDIMMs) built with x4 and x8 devices, load-reduced DIMMs (LRDIMMs) built with dual-die and stacked packages, and three-dimensional stacked DIMMs (3DS DIMMs).

Table 1. Supported Standard DIMM Types on AMD EPYC 7002 Processors

DIMM Type	Ranks	Capacity **
RDIMM	1 (SR)	8 GB, 16 GB, or 32 GB
RDIMM	2 (DR)	16 GB, 32 GB, or 64 GB
LRDIMM	4	64 GB or 128 GB
LRDIMM	8	128 GB or 256 GB
3DS	4	64 GB or 128 GB
3DS	8	128 GB or 256 GB

*This table represents a listing of DIMMs available on AMD EPYC 7002 processors at the time of writing. While the AMD EPYC 7001 processor is compatible with the listed DIMM configurations, you should consult with your platform vendor for a list of supported DIMMs.

** See Appendix A “DIMM Population Rules” for guidance on mixing different DIMMs

Reference Documents

PID	Title
55803	<i>Processor Programming Reference (PPR) for AMD Family 17h Models 30h-3Fh Processors</i>
56338	<i>Socket SP3 Platform NUMA Topology for AMD Family 17h Models 30h-3Fh</i>

Memory Bandwidth

AMD EPYC 7002 processors have eight memory channels, designated A, B, C, D, E, F, G, and H. Each channel supports up to two DIMMs. Systems can be built with one DIMM per channel (1 DPC), two DIMMs per channel (2 DPC), or a combination thereof.

The operating speed of memory will depend on the number and types of DIMMs in the system, as well as the specific type of motherboard used. There are two types of motherboards defined. These have different characteristics in terms of the memory and I/O subsystem, as well as the system thermal design power (TDP) capability. Boards designed for the AMD EPYC 7001 processors will accommodate AMD EPYC 7002 processors as a system compatible, drop-in upgrade. These boards are designated Motherboard Type-0 boards and are constrained to operate at the AMD EPYC 7001 processor’s memory and I/O speeds. An alternate motherboard design, which is not necessarily compatible with AMD EPYC 7001 processors, unlocks the full capability of AMD EPYC 7002 processors, including higher speed memory and I/O devices. This is designated Motherboard Type-1. Table 2 illustrates the differences between the two.

While a decreased operational frequency with two DIMMs populated may not seem ideal for memory-intensive workloads, the additional chip selects being used, or ranks of memory, can outweigh the change in operating memory speed in certain workloads.

Table 2. EPYC Memory Speed based on DIMM Population (One DIMM per Channel)

DIMM Type	DIMM Population	DDR4 Frequency MT/s	
	DIMM 0	AMD EPYC 7002 processors in Legacy Platforms (Type-0 Motherboards)	AMD EPYC 7002 processors in Optimized Platforms (Type-1 Motherboards)
RDIMM	1R (one rank)	2666	3200
	2R or 2DR (two ranks)	2666	3200
LRDIMM	4DR (four ranks)	2666	3200
	2S2R (four ranks)	2666	3200
	2S4R (eight ranks)	2666	3200
3DS	2S2R (four ranks)	2666	3200
	2S4R (eight ranks)	2666	3200

Table 3. EPYC Memory Speed based on DIMM Population (Two DIMMs per Channel)

DIMM Type	DIMM Population/Channel		DDR4 Frequency (MT/s)	
	DIMM 0	DIMM 1	AMD EPYC 7002 processors in Legacy Platforms (Type-0 Motherboards)	AMD EPYC 7002 processors in Optimized Platforms (Type-1 Motherboards)
RDIMM	–	1R	2666	3200
	1R	1R	2133	2933
	–	2R or 2DR	2400	3200
	1R	2R or 2DR	2133	2933
	2R or 2DR	2R or 2DR	2133	2933
LRDIMM	–	4DR	2666	3200
	4DR	4DR	2133	2933
	–	2S2R (4 ranks)	2666	3200
	–	2S4R (8 ranks)	2666	3200
	2S2R (4 ranks)	2S2R (4 ranks)	2133	2933
	2S4R (8 ranks)	2S4R (8 ranks)	2133	2933
3DS	–	2S2R (4 ranks)	2400	2933
	2S2R (4 ranks)	2S2R (4 ranks)	1866	2666
	–	2S4R (8 ranks)	2400	2933
	2S4R (8 ranks)	2S4R (8 ranks)	1866	2666

Choosing the Right Configuration

AMD recommends that all eight memory channels per CPU socket be populated with each channel having equal capacity. This enables the memory subsystem to operate in eight-way interleaving mode, which should provide the best performance in most cases.

For a given processor model number, memory population, and NUMA node per socket (NPS) configuration, the pre-BIOS firmware chooses the optimal memory interleaving option. There are three NPS options available: NPS=1, NPS=2, and NPS=4. These are described in more detail in “*Socket SP3 Platform NUMA Topology for AMD Family 17h Models 30h-3Fh*”.

The following diagrams are examples of supported DIMM configurations in a system. Notice, however, that most configurations populating fewer than eight channels are supported, but not recommended. For a full list of population and interleaving rules, refer to Appendix A: DIMM Population Rules. For a matrix of supported memory, refer to Appendix B: Memory Population Topologies.

Four DIMM Configuration (Conditionally Recommended only with EPYC processors that have 128MB L3 or less¹)

Interleave: CDGH (NPS=1; default and preferred)

Other interleave options: CD, GH (NPS=2)

All DIMM have the same capacity

DIMM are unpopulated

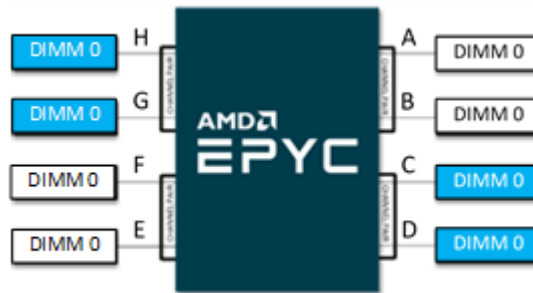


Figure 1. Example: Four DIMM Population in 1 DPC Configuration

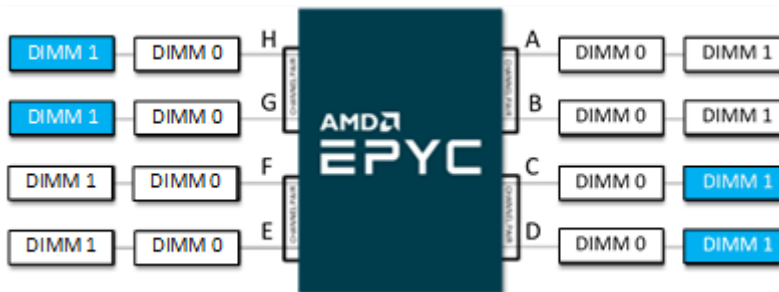


Figure 2. Example: Four DIMM Population in 2 DPC Configuration

¹ Recommended only if eight channels cannot be populated and only with processors that have 128MB L3 or less

Eight DIMM Configuration (Recommended)

Interleave: ABCDEFGH, NUMA Nodes Per Socket (NPS)=1 (default and preferred)

Other interleave options: ABCD, EFGH (NPS=2) and AB, CD, EF, GH (NPS=4)

All DIMM 0 have the same capacity

DIMM are unpopulated

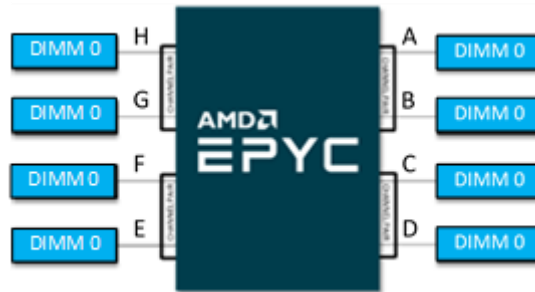


Figure 3. Example: Eight DIMM Population in 1 DPC Configuration

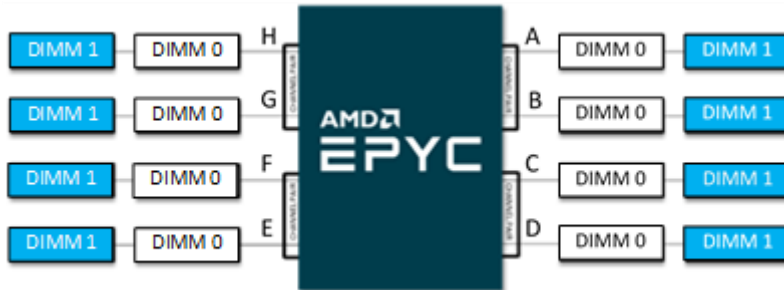


Figure 4. Example: Eight DIMM Population in 2 DPC Configuration

Ten DIMM Configuration (Recommended)

Interleave: ABCDEFGH, NUMA Nodes Per Socket (NPS)=1 (default and preferred)

Other interleave options: ABCD, EFGH (NPS=2) and AB, CD, EF, GH (NPS=4)

DIMM = 2x capacity of DIMM

All DIMM have the same capacity

DIMM are unpopulated

Two DIMMs occupying the same channel are of the same type

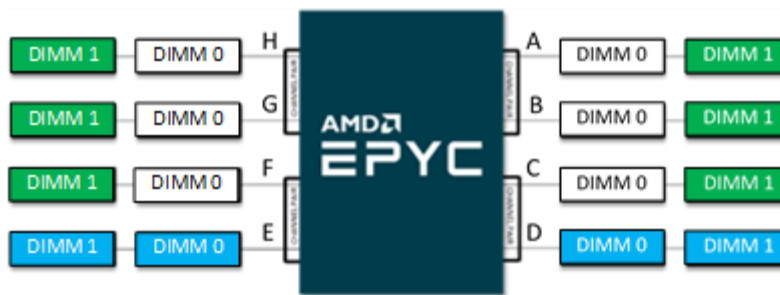


Figure 5. Example: Ten DIMM Population in 2 DPC Configuration

Twelve DIMM Configuration (Recommended)

Interleave: ABCDEFGH, NUMA Nodes Per Socket (NPS)=1 (default and preferred)

Other interleave options: ABCD, EFGH (NPS=2) and AB, CD, EF, GH (NPS=4)

DIMM = 2x capacity of DIMM

All DIMM have the same capacity

DIMM are unpopulated

Two DIMMs occupying the same channel are of the same type

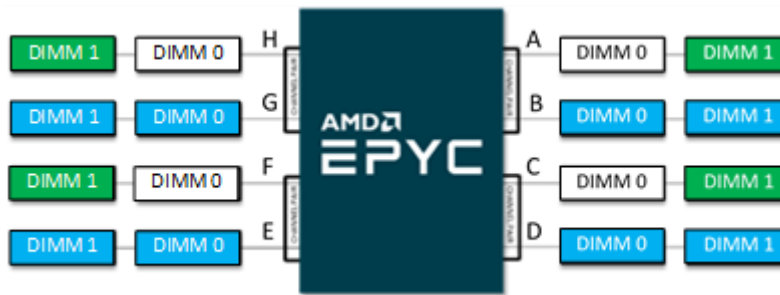


Figure 6. Example: Twelve DIMM Population in 2 DPC Configuration

Fourteen DIMM Configuration (Recommended)

Interleave: ABCDEFGH, NUMA Nodes Per Socket (NPS)=1 (default and preferred)

Other interleave options: ABCD, EFGH (NPS=2) and AB, CD, EF, GH (NPS=4)

DIMM = 2x capacity of DIMM

All DIMM have the same capacity

DIMM are unpopulated

Two DIMMs occupying the same channel are of the same type

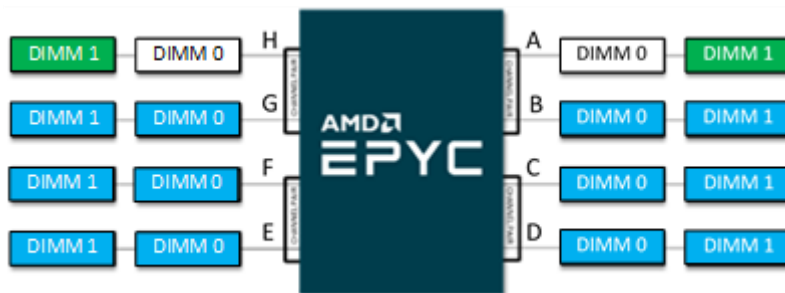


Figure 7. Example: Fourteen DIMM Population in 2 DPC Configuration

Sixteen DIMM Configuration (Recommended)

Interleave: ABCDEFGH, NUMA Nodes Per Socket (NPS)=1 (default and preferred)

Other interleave options: ABCD, EFGH (NPS=2) and AB, CD, EF, GH (NPS=4)

All DIMM have the same capacity

Two DIMMs occupying the same channel are of the same type

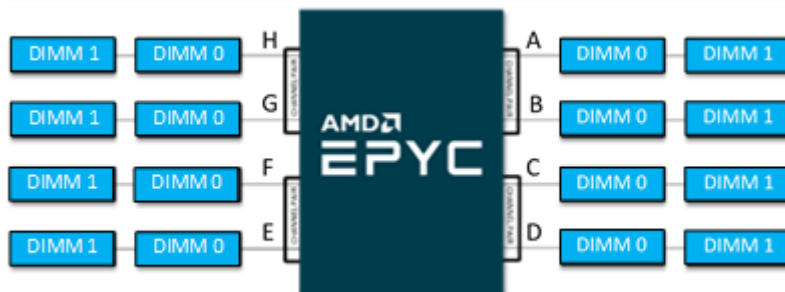


Figure 8. Example: Sixteen DIMM Population in 2 DPC Configuration

Appendix A: DIMM Population Rules

- Supported device technology:
 - DDR4 8 Gbit, 16 Gbit.
- Supported DIMM types²:
 - 1R and 2R RDIMM, built with x4 and x8 DDR4 devices.
 - 4R and 8R LRDIMM, built with x4 DDR4 devices (4DR, 2S2R, 2S4R devices).
 - 2S2R (= 4R) and 2S4R (= 8R) 3DS built with x4 DDR4 devices.
- Unsupported DIMM types:
 - UDIMMs, 4R RDIMMs.
- General population order guidelines
 - Populate open channels before populating two DIMMs on a given channel
 - In 2 DPC configurations where only one DIMM is populated on a channel, populate the DIMM socket physically farthest away from the processor.
 - Balance memory capacity per channel pair on a given processor
 - Balance memory capacity per processor socket in a two-socket system.
 - Though a system can be populated with a single DIMM as a minimum configuration, full memory bandwidth requires one DIMM per channel (A–H) be populated
 - ▲ **For best performance, AMD recommends populating all eight memory channels per socket, with every channel having the same capacity.**
 - ▲ If a customer chooses to populate only four channels in the system, AMD recommends limiting the processors in that system to those with 128MB or less of L3 and populating channels CDGH identically. This will enable four-way interleaving, which will generally provide the best performance with a four DIMM population.
- General population rules:
 - RDIMM, LRDIMM, and 3DS DIMM types can coexist in the system with restrictions.
 - DIMMs within the same socket must be of the same base DIMM module type. No mixing RDIMM, LRDIMM, or 3DS on a socket.
 - DIMMs within the same channel must be of the same DRAM width. No mixing DIMMs with x4 and x8 DRAMs on a channel.

² **4DR** = Four ranks of dual die packaged DRAM.

2S2R = Two ranks of two high stacked 3DS DRAM. Four ranks total.

2S4R = Two ranks of four high stacked 3DS DRAM. Eight ranks total.

- DIMMs within the same channel must be of the same DRAM density. No mixing DIMMs with 8Gb and 16Gb DRAMs on a channel.
 - While DIMMs with different manufacturers can be populated on the same channel, platform developers are expected to validate these configurations.
 - All memory channels operate at the same frequency. The system will use the highest common supported frequency when populated with different speed DIMMs. The highest common supported speed is the rated speed of the slowest DIMM in the system while also applying the population speed limits for the configuration (1 of 1, 1 of 2, 2 of 2).
- o General interleaving rules
- Memory channels may be organized in four pairs: A+B, C+D, E+F, and G+H. These pairs may be interleaved together (two-way interleaving), a specific set of two pairs may be interleaved together (four-way interleaving like CDGH), or all channels may be interleaved together (ABCDEFGH).
 - ▲ Eight-way interleaving is only possible when all eight channels are populated with equal size memory and NPS=1.
 - ▲ Four-way interleaving when NPS=1 is only possible when channels CDGH are populated with equal size memory, and no other channels are populated.
 - ▲ Four-way interleaving when NPS=2 is only possible when channels ABCD and EFGH are populated with equal size memory. It is possible to have 2 four-way interleaves of ABCD and EFGH simultaneously if channels ABCD are all equal size memory, and channels EFGH are all equal size memory. The memory sizes of ABCD and EFGH are independent of each other in this case and can be different.
 - ▲ Two-way interleaving when NPS=2 is only possible when channels CD and GH are populated with equal size memory and no other channels are populated.
 - ▲ Two-way interleaving is also possible for channels AB, CD, EF, and GH for NPS=4. For an optimized configuration, each channel in a pair of channels should have identical capacity. While supported, unequal capacity configurations are suboptimal because the larger DIMM's excess capacity will not be interleaved, resulting in only the matched memory capacity between the DIMMs being interleaved.
 - ▲ When two identical DIMMs are populated in a channel, chip select interleaving across those DIMMs in the channel can be enabled.
 - The resulting interleave is based on the processor model number, how the DIMMs are populated in the system, and the chosen NPS value.
 - While DIMMs with different ranks (1R/2R) in the same channel or channel pair are supported, the resulting interleave may not have optimal performance.

Appendix B: Memory Population Topologies

Nomenclature

M_n: represents the total memory capacity in the indicated channel. The channel can be comprised of one or two DIMMs.

- ABCDEFGH: one block of eight-way interleaved memory. The capacity of all channels must be equal.
- ABCD, EFGH: two blocks of four-way interleaved memory. The capacity of channels ABCD must be equal and the capacity of EFGH must be equal.
- AB, CD, EF, GH: four blocks of two-way interleaved memory. The interleave across each channel in a channel pair occurs across the capacity in common to the two channels.
- AB, CD, E, GH: three blocks of two-way interleaved memory and one block of non-interleaved memory.

How to Use

This table is a listing of sample legal memory populations in the system and resultant interleave for the NUMA nodes per socket (NPS) selected for that system. This is not an exhaustive listing of every possible memory configuration but should demonstrate what is involved when selecting the optimal memory population in a system.

The first column indicates the number of memory channels populated with DIMMs. It does not indicate the number of DIMMs in the channel. There can be one or two DIMMs per channel. For example, a 12 DIMM configuration that populates all memory channels, six of which have one DIMM per channel and two of which have two DIMMs per channel fall under the eight channels populated rows.

The M1–M4 nomenclature indicates total memory capacity on a given channel and that those channels can be interleaved per the rules defined in Appendix A. That capacity can be from a single DIMM or two DIMMs on the channel. For example, channel A with a single DIMM is designated to have capacity M1. If channel B has two DIMMs, each with half the capacity of the DIMM on channel A, channel B will also be labeled with M1.

Table 4. Memory Matrix Topologies

# Channels populated (with 1 or 2 DIMMs/ch)	Memory Channel								Interleave for selected NPS						Notes	
	M = total DIMM capacity on indicated channel and can be one or two DIMMs.								NPS=1		NPS=2		NPS=4			
	A	B	C	D	E	F	G	H								
4	<empty>	<empty>	M1	M1	<empty>	<empty>	M1	M1	CDGH	CD	GH	<null>	CD	<null>	GH	2
4	M1	M1	M1	M1	<empty>	<empty>	<empty>	<empty>	AB, CD	ABCD	<null>	AB	CD	<null>	<null>	2
4	<empty>	<empty>	<empty>	<empty>	M1	M1	M1	M1	EF, GH	<null>	EFGH	<null>	<null>	EF	GH	2
8	M1	M1	M1	M1	M1	M1	M1	M1	ABCDEFGH	ABCD	EFGH	AB	CD	EF	GH	3
8	M2	M2	M1	M2	M2	M2	M2	M2	AB, C, D, EF, GH	AB, C, D	EF, GH	AB	C, D	EF	GH	1
8	M2	M2	M1	M1	M2	M2	M2	M2	AB, CD, EF, GH	AB, CD	EF, GH	AB	CD	EF	GH	1
8	M2	M2	M1	M1	M2	M2	M1	M2	AB, CD, EF, G, H	AB, CD	EF, G, H	AB	CD	EF	G, H	1
8	M1	M1	M1	M1	M2	M2	M2	M2	AB, CD, EF, GH	ABCD	EFGH	AB	CD	EF	GH	4
8	M1	M1	M2	M2	M1	M1	M2	M2	AB, CD, EF, GH	AB, CD	EF, GH	AB	CD	EF	GH	1
8	M2	M2	M1	M3	M3	M3	M3	M3	AB, C, D, EF, GH	AB, C, D	EF, GH	AB	C, D	EF	GH	1
8	M2	M2	M2	M2	M1	M1	M3	M3	AB, CD, EF, GH	AB, CD	EF, GH	AB	CD	EF	GH	1
8	M1	M1	M2	M2	M3	M3	M4	M4	AB, CD, EF, GH	AB, CD	EF, GH	AB	CD	EF	GH	1

Notes

- 1: This is an sample channel population for the given number of channels populated. It is intended to show how interleaving can be affected by channel population. Due to the disparate channel population in the example, performance is limited to two-way interleaving for all configurations. For instance, in the 1 channel population row, only channel A is shown as being populated but it could be populated in any other channel instead with similar interleaving performance. It is recommended to populate channel pairs with identical DIMMs wherever possible for optimal performance.
- 2: Four-way interleaving is possible for ABCD, EFGH, or CDGH populations, with CDGH having the best performance. Recommended only if eight channels cannot be populated, and only with processors that have 128MB or less of L3 per socket. All populated channels must have equal capacity.
- 3: Eight-way interleaving is possible for ABCDEFGH population when they have equal capacity. This is the recommended channel population for best performance in all cases.
- 4: Dual four-way interleaving is possible in this configuration for NPS=2 only. The capacity of channels ABCD must be the same, and the capacity of channels EFGH must be the same, but the capacity of ABCD does not have to equal the capacity of EFGH.