Memory Population Guidelines for AMD EPYC™ Processors

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Advanced Micro Devices

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Revision History

Date	Revision	Description
September 2018	1.1	Added clarification on usage of different bus-width memory.
July 2018	1.0	Initial public release.

Introduction

The AMD EPYC™ processor is designed with an industry leading eight channels of DDR4 memory per x86 processor. With more memory channels, users will have fewer memory bottlenecks, and better performance for memory bound workloads. Every processor part number includes support for all eight memory channels and supports the same DIMM types which include registered (RDIMMs) and load reduced DIMMs (LRDIMMs).

Table 1. Supported DIMM Types on AMD EPYC™ Processors

DIMM Type	Ranks	Capacity [1, 2]
RDIMM	1 (SR)	8 GB
RDIMM	1 (SR)	16 GB
RDIMM	2 (DR)	16 GB
RDIMM	2 (DR)	32 GB
LRDIMM	4	64 GB
LRDIMM	8	128 GB

[1] This table is a representative listing of DIMMs available on AMD EPYC processors at the time of writing. While the AMD EPYC Naples family of processors is compatible with the listed DIMM configurations, it is recommended that you consult with your platform vendor for a list of supported DIMMs.

[2] While EPYC supports multiple ranks (1R, 2R, 4R, 8R), different data-bus widths of each DRAM on the same channel are not supported. If a need arises to replace an existing memory module (e.g. 2Rx8) you must match the given designation or replace the entire bank with the new type.

Memory Bandwidth

There are 13 total AMD EPYC processor part numbers that support different maximum DDR frequencies. The memory frequencies used will dictate the max TDP of the system for those part numbers where two TDPs are provided.

Table 2. Available AMD EPYC™ Processor Configurations

Part Number	Single/Dual Socket	Cores	Max DDR Frequency (MHz)	TDP (W)
7601	1P or 2P	32	2666	180
7551	1P or 2P	32	2666	180
7551P	1P only	32	2666	180
7501	1P or 2P	32	2400/2666	155/170
7451	1P or 2P	24	2666	180
7401	1P or 2P	24	2400/2666	155/170
7401P	1P only	24	2400/2666	155/170
7351	1P or 2P	16	2400/2666	155/170
7351P	1P only	16	2400/2666	155/170
7301	1P or 2P	16	2400/2666	155/170
7281	1P or 2P	16	2400/2666	155/170
7261	1P or 2P	8	2400/2666	155/170
7251	1P or 2P	8	2400	120

Memory channels are organized in pairs (e.g. A and B are a channel pair). To achieve optimal memory performance, populate the memory in the following order:

- Populate open channels before populating two DIMMs on a given channel
- Though a system can be populated with a single DIMM as a minimum configuration
  - Full memory bandwidth requires one DIMM per channel (A-H) be populated
  - Minimum recommended: At least one DIMM is populated for each channel pair in the system (A,C,E,G)
- Balance memory capacity per channel pair on a given CPU
- In a two-socket system, if two CPUs are populated, balance memory capacity between them

The operating speed of memory will depend on the type of DIMM and population configuration, however, if a 2400 MHz or 2666 MHz DIMM is populated in both DIMM slots on a channel the frequency on both will drop to 2133 MHz. Some OEM vendors will support two DIMMs per channel, for a total of 16 DIMMs per socket, while due to space constraints or platform requirements others will support one DIMM per channel, for a total of eight DIMMs per socket. Below you will find a graphic for reference of these two configurations.

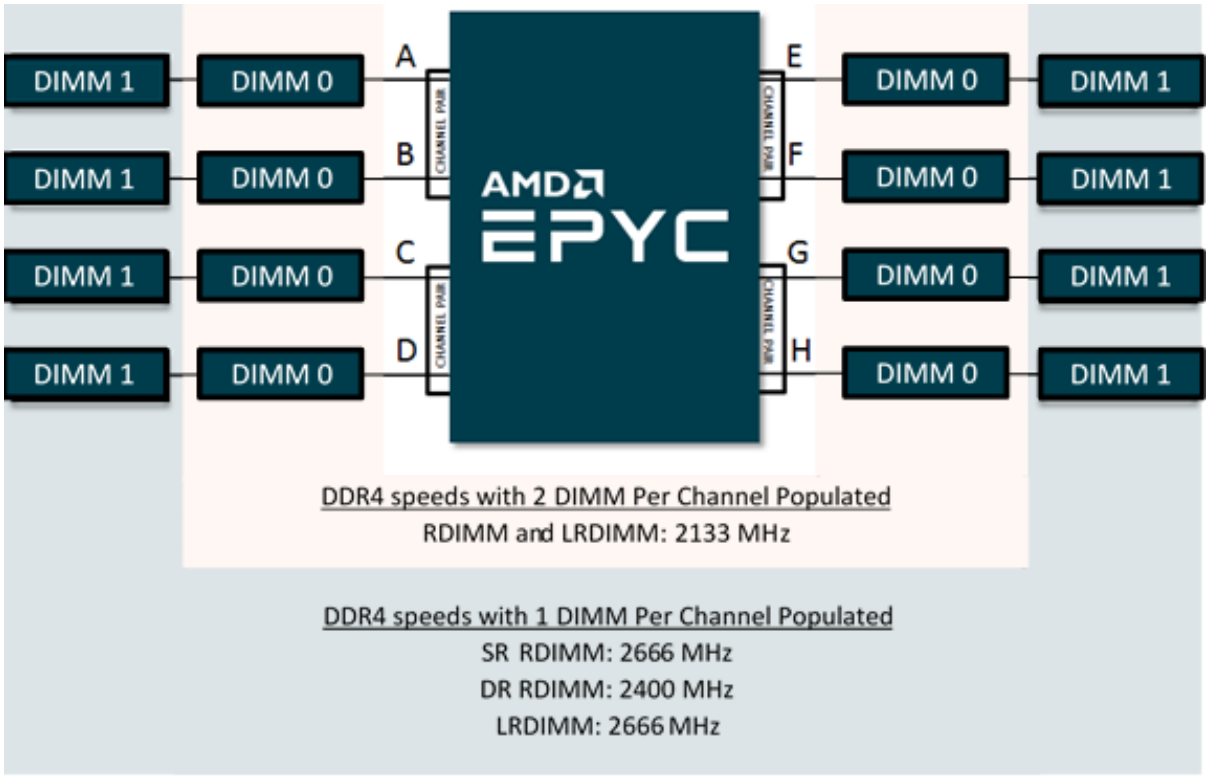


Figure 1. Operational DDR4 Speeds Based on DIMM Population in a Two DIMM Per Channel Configuration

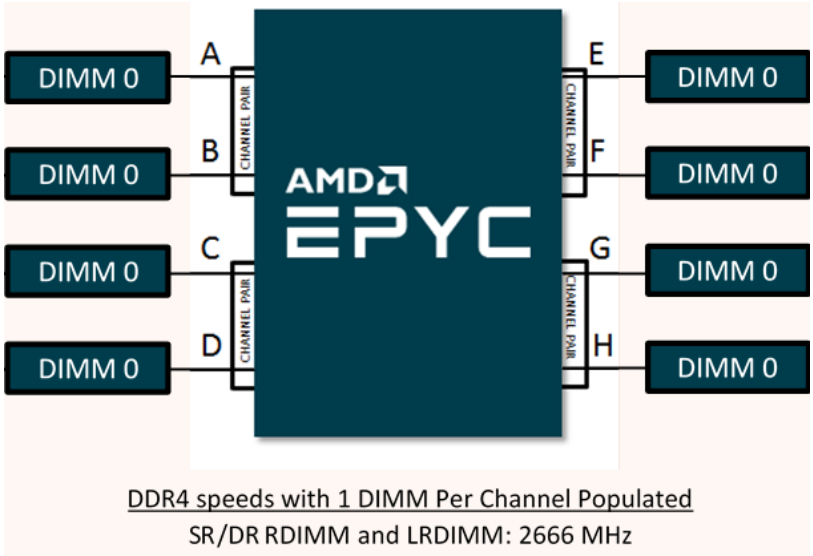


Figure 2. Operational DDR4 Speeds Based on DIMM Population in a Single DIMM Per Channel Configuration

While it may seem that a decreased operational frequency with two DIMMs populated is not ideal for memory intensive workloads, the additional chip selects being used, or ranks of memory, can outweigh the change in operating memory speed in certain workloads.

Table 3. Theoretical Bandwidth per Channel at a Given Transfer Rate[i]

DIMM Operational Frequency	Theoretical Bandwidth per Channel
DDR4 @ 2133 MHz	17 GB/s
DDR4 @ 2400 MHz	19.2 GB/s
DDR4 @ 2666 MHz	21.3 GB/s

Table 4. EPYC Memory Speed based on DIMM Population

Memory Population	Memory Speed
2 DIMMs per Channel	8 x DDR4 @ 2133 MHz = 136 GB/s
1 DIMM per Channel DR	8 x DDR4 @ 2400 MHz = 154 GB/s
1 DIMM per Channel SR or LRDIMM	8 x DDR4 @ 2666 MHz = 170 GB/s

Choosing the Right Configuration

General Performance and Capacity: Balanced for Bandwidth, Capacity, and Cost

A large portion of datacenter workloads will benefit from the balance, cost, and performance of populating the system with one DIMM per channel using Dual Rank (DR) RDIMMs. Eight channels of memory, and eight 32GB DR RDIMMs will yield 256 GB per CPU of memory capacity and industry leading max theoretical memory bandwidth of 154 GB/s.

Some core performance bound workloads may benefit from this configuration as well.

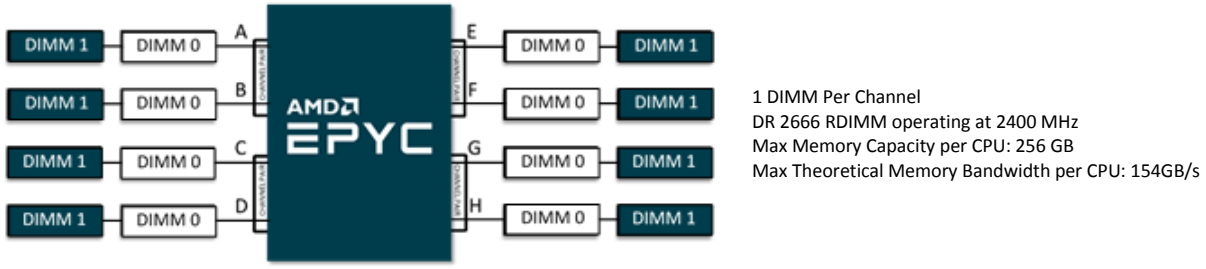
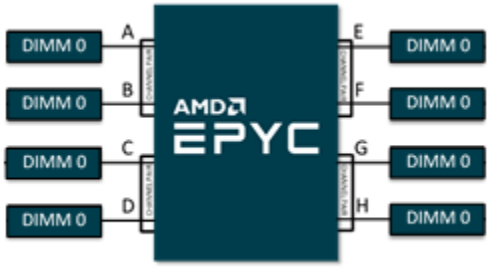


Figure 3. Sample Configuration for Balance of Bandwidth, Capacity and Cost

Memory Bandwidth Sensitive Workloads

Memory bound workloads will benefit from the maximum available memory speed. This can be achieved with one 2666 MHz DIMM per channel in a single slot per channel platform. This configuration would be beneficial in memory bound high-performance computing (HPC) workloads such as: computational fluid dynamics (CFD), weather modeling, crash simulation, and oil and gas (O&G) exploration.

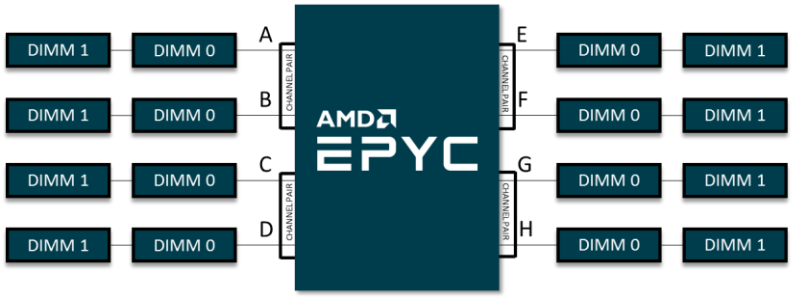


1 DIMM Per Channel
SR/DR RDIMM or LRDIMM operating at 2666 MHz
Max Memory Capacity per CPU: 512 GB
Max Theoretical Memory Bandwidth per CPU: 170GB/s

Figure 4. Sample Configuration for Memory Bandwidth Sensitive Workloads

Cost Effective Memory Capacity

Workloads that benefit from large memory capacity footprints will benefit from populating both DIMMs on a given channel. Using 16 32GB DR RDIMMs will provide 512GB of memory per CPU.



2 DIMMs Per Channel
DR 2666 RDIMM operating at 2133 MHz
Max Memory Capacity per CPU: 512 GB
Max Theoretical Memory Bandwidth per CPU: 136GB/s

Figure 5. Sample Configuration for Cost Effective Memory Capacity

Maximum Memory Capacity

To achieve the maximum memory capacity per CPU, populate both DIMM slots with 16 128GB LRDIMMs. This configuration will provide a total of 2TB of memory per CPU.

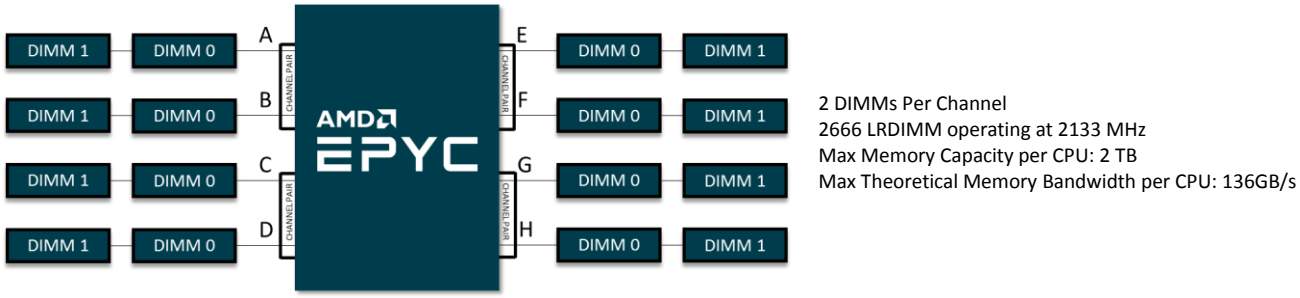


Figure 6. Sample Configuration for Maximum Memory Capacity

Minimum Supported

An AMD EPYC processor-based system is capable of functioning with a single DIMM, regardless of memory type, however, it is recommended that systems be populated with at least one DIMM per channel pair.

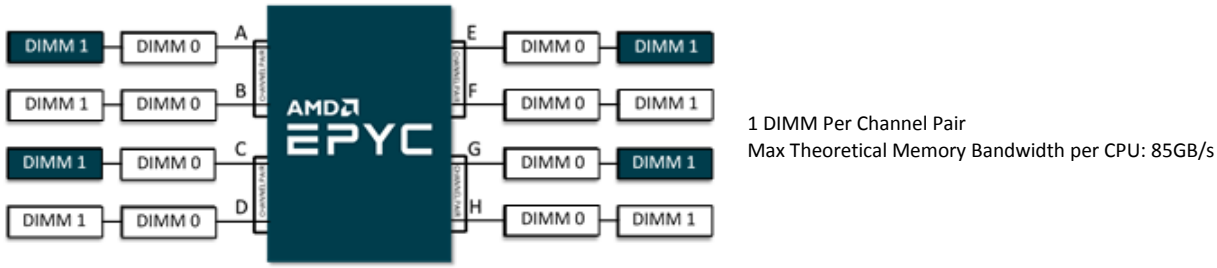


Figure 7. Minimum Supported Configuration

[i] *https://en.wikipedia.org/wiki/DDR4_SDRAM*