AMD-8111™ HyperTransport™ I/O Hub Revision Guide

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Trademarks

Revision History

Date	Rev	Description
March 2006	3.13	Added erratum #63.
February 2005	3.11	Added erratum #62
November 2004	3.09	Added erratum #61.
April 2004	3.07	Added erratum #58–60.
September 2003	3.05	Added erratum #57.
July 2003	3.03	Changed all C2 silicon errata Fix Planned status to “No”.
April 2003	3.00	Initial public release.

AMD-8111™ HyperTransport™ I/O Hub Revision Guide

The purpose of the *AMD-8111™ HyperTransport™ I/O Hub Revision Guide* is to communicate updated product information on the AMD-8111™ HyperTransport™ I/O hub to designers of computer systems and software developers. This guide consists of three major sections:

- **Revision Determination:** This section, starting on page 6, describes the mechanism by which the current revision of the part is identified.
- **Product Errata:** This section, starting on page 7, provides a detailed description of product errata, including potential effects on system operation and suggested workarounds. An erratum is defined as a deviation from the product's specification. A product errata may cause the behavior of the AMD-8111 HyperTransport I/O hub to deviate from the published specifications.
- **Documentation Support:** This section, starting on page 31, provides a listing of available technical support resources.

Revision Guide Policy

Occasionally, AMD identifies product errata that cause the AMD-8111 HyperTransport I/O hub to deviate from published specifications. Descriptions of identified product errata are designed to assist system and software designers in using the AMD-8111 HyperTransport I/O hub. This revision guide may be updated periodically.

Revision Determination

The BIOS checks the PCI revision ID register for function 0h at offset 8h to determine the version of silicon as shown in Table 1.

Table 1. AMD-8111™ HyperTransport™ I/O Hub Revision IDs

Sequence	Revision	Device A Function 0h Offset 8h
6	C2	07h

Product Errata

This section documents AMD-8111™ HyperTransport™ I/O hub product errata. A unique tracking number for each erratum has been assigned within this document for user convenience in tracking the errata within specific revision levels. Table 2 cross-references the revisions of the part to each erratum. An "X" indicates that the erratum applies to the revision. The absence of an "X" indicates that the erratum does not apply to the revision.

Note: *There may be missing errata numbers. Errata that have been resolved from early revisions of the device have been deleted, and errata that have been reconsidered may have been deleted or renumbered.*

Table 2. Cross-Reference of Product Revision to Errata

Errata Numbers and Description	Revision Number
	C2
9 USB 2.0 High-Speed Traffic is Not Supported	X
33 DevB:3x43[VDDA_STS] Set Erroneously	X
34 RTC RAM Valid Bit Not Updated Correctly	X
36 Watchdog Timer is Not Functional	X
38 PM1C[ARB_DIS] Blocks System Management Messages	X
42 Peer-to-Peer Posted Requests to the AMD-8111™ HyperTransport™ I/O Hub Secondary PCI Bus May Cause System to Hang	X
44 AMD-8111™ HyperTransport™ I/O Hub Does Not Support Fast Back-to-Back PCI Transactions	X
47 PCI Posted Request Master Abort Does Not Generate HyperTransport™ Technology Sync Flood	X
48 PCI Posted Request Target Abort Does Not Generate HyperTransport™ Technology Sync Flood	X
49 PERR# Assertion Does Not Generate HyperTransport™ Technology Sync Flood	X
52 Some PCI Prefetching Control Settings Cause PCI Bus Performance to Degrade	X
53 VDD_RTC Current in G3 May Exceed 8 μA Maximum	X
54 USB in Reset Following Exit from S3 State	X
55 Non-Posted Starvation Scenario with IDE or EHCI Controller	X
56 DevB:3x64[5] Always Returns 0	X
57 PCI Input Hold Time Violation	X
58 Subtractive Decode Routing to the PCI Bus Not Supported	X
59 LPC Input Hold Time Violation	X
60 CMOS Lock Control	X
61 I/O and LPC DMA Conflict	X

Table 2. Cross-Reference of Product Revision to Errata (continued)

62 Downstream Posted Write Completion Dependency On Upstream Posted Write Completion	X
63 AMD-8111™ HyperTransport™ I/O Hub Lacks Extended Configuration Space Memory-Mapped I/O Base Address Register	X

9 USB 2.0 High-Speed Traffic is Not Supported

Description
The internal USB controllers do not support USB 2.0 high-speed traffic in some revisions of the AMD-8111 HyperTransport I/O hub.

Potential Effect on System
Devices that support only USB 2.0 high-speed traffic cannot connect to the I/O hub.

Suggested Workaround
Use an external USB 2.0 controller to support USB 2.0 functionality.

Fix Planned
No

33 DevB:3x43[VDDA_STS] Set Erroneously

Description
The value of DevB:3x43[VDDA_STS] may become set erroneously when the system transitions from the ACPI G3 state to the ACPI S0 or S5 state.

Potential Effect on System
DevB:3x43[VDDA_STS] incorrectly reports that VDD_COREAL and VDD_IOAL lost power, and system software initializes the contents of the AMD-8111 HyperTransport I/O hub internal battery-powered RAM with default values.

Suggested Workaround
System firmware must not evaluate DevB:3x43[VDDA_STS] but instead should use a checksum calculation to determine whether the data in the battery-powered RAM has become inconsistent.

Contact your AMD technical representative for further information about system firmware revisions.

Fix Planned
No

34 RTC RAM Valid Bit Not Updated Correctly

Description
The real time clock (RTC)RAM Valid bit at RTC register offset 0Dh bit 7 may not be updated correctly when VDD_RTC is not powered.

Potential Effect on System
The RTC RAM Valid bit can not be used to determine that VDD_RTC is not powered.

Suggested Workaround
System firmware must not evaluate the RAM Valid bit but instead should use a checksum calculation to determine whether the data in the battery powered RAM has become inconsistent.

Contact your AMD technical representative for further information about system firmware revisions.

Fix Planned
No

36 Watchdog Timer is Not Functional

Description
The AMD-8111 HyperTransport I/O hub internal watchdog timer registers DevB:0xA8, WDT00, and WDT08 are not accessible. Write operations to those registers are discarded. Read operations to DevB:0xA8 return all zeros. Read operations to WDT00 and WDT08 return all ones.

Potential Effect on System
None expected. The watchdog timer provides additional functionality for platform management. It is not required for normal operations.

Suggested Workaround
None required.

Fix Planned
No

38 PM1C[ARB_DIS] Blocks System Management Messages

Description
When PM1C[ARB_DIS] is set, system management messages from the AMD-8111 HyperTransport I/O hub to the host are blocked by the I/O hub internal message controller.

Potential Effect on System
The system hangs under the following conditions:

1. System software sets PM1C[ARB_DIS] in order to prepare the system to transition into the ACPI C3 state.
2. System software reads PM15 in order to transition the system into the ACPI C3 state.

When the above conditions occur, the STPCLK-assertion system management message to the host, in response to the read request to PM15, is blocked by the I/O hub internal message controller. Subsequently, the read response for the read request to PM15 is blocked since a read response is not allowed to pass a posted system management message. Thus, the system hangs.

Suggested Workaround
Do not set PM1C[ARB_DIS]. Clear DevB:3x4F[C3EN] to prevent the system from transitioning into the ACPI C3 state.

Fix Planned
No

42 Peer-to-Peer Posted Requests to the AMD-8111™ HyperTransport™ I/O Hub Secondary PCI Bus May Cause System to Hang

Description
Long sequences of peer-to-peer posted requests to the I/O hub secondary PCI bus may cause the system to hang under the following conditions:

1. A bus master on the I/O hub secondary PCI bus generates a long sequence of posted requests to system memory.
2. A read request from the host to the LPC bus or some I/O hub internal address space is received by the I/O hub.
3. A bus master on a bus segment of a HyperTransport tunnel device, which is part of the same HyperTransport chain as the I/O hub, generates a long sequence of posted requests to the I/O hub secondary PCI bus.

Under these conditions, neither of the transactions may be able to make progress. Thus, the system hangs.

Potential Effect on System
System hangs and recovers only after a hardware reset is generated.

Suggested Workaround
Place the source and sink device of peer-to-peer transactions on the same bus segment (e.g., the I/O hub secondary PCI bus).

Fix Planned
No

44 AMD-8111™ HyperTransport™ I/O Hub Does Not Support Fast Back-to-Back PCI Transactions

Description
Fast back-to-back transactions to the AMD-8111 HyperTransport I/O hub cause the system to hang.

DevA:0x1C[23] indicates that the I/O hub does not support fast back-to-back transactions to different targets on the secondary PCI bus. Therefore, per the *PCI Local Bus Specification*, system software is required to disable the generation of fast back-to-back transactions (to different targets) from any bus master on the secondary PCI bus. Although it is allowed by the PCI specification, there are currently no known PCI masters that generate fast back-to-back transactions to the same target (i.e., the I/O hub) when fast back-to-back transactions to different targets have been disabled.

Potential Effect on System
The system hangs.

Suggested Workaround
None required.

Fix Planned
No

47 PCI Posted Request Master Abort Does Not Generate HyperTransport™ Technology Sync Flood

Description
When a posted request from the host to a target on the secondary PCI bus of the AMD-8111 HyperTransport I/O hub is terminated with a master abort and DevA:3C[MARSP] is set, the I/O hub sets DevA:0x1C[RMA] but fails to generate a sync flood on its HyperTransport transmit link when DevA:0x04[SERREN] is set.

Potential Effect on System
None expected for systems that do not enable the generation of sync flood. For systems that enable the generation of sync flood, the I/O hub fails to signal the master abort by sync flood.

Suggested Workaround
None required for systems that do not require the detection of a master abort. For systems that require the detection of a master abort, set DevB:0x40[NMIONERR] to enable the generation of an NMI when DevA:0x1C[RMA] is set.

Fix Planned
No

48 PCI Posted Request Target Abort Does Not Generate HyperTransport™ Technology Sync Flood

Description
When a posted request from the host to a target on the secondary PCI bus of the AMD-8111 HyperTransport I/O hub is terminated with a target abort, the I/O hub sets DevA:0x1C[RTA] but fails to generate a sync flood on its HyperTransport transmit link when DevA:0x04[SERREN] is set.

Potential Effect on System
None expected for systems that do not enable the generation of sync flood. For systems that enable the generation of sync flood, the I/O hub fails to signal the target abort by sync flood.

Suggested Workaround
None required for systems that do not require the detection of a target abort. For systems that require the detection of a target abort, set DevB:0x40[NMIONERR] to enable the generation of an NMI when DevA:0x1C[RTA] is set.

Fix Planned
No

49 PERR# Assertion Does Not Generate HyperTransport™ Technology Sync Flood

Description
When PERR# is asserted during a posted request from the host to a target on the secondary PCI bus of the AMD-8111 HyperTransport I/O hub and DevA:0x3C[PEREN] is set, the I/O hub sets DevA:0x1C[MDPE] but fails to generate a sync flood on its HyperTransport transmit link when DevA:0x04[SERREN] is set.

Potential Effect on System
None expected for systems that do not enable the generation of sync flood. For systems that enable the generation of sync flood, the I/O hub fails to signal the assertion of PERR# by sync flood.

Suggested Workaround
None required for systems that do not require the detection of PERR#. For systems that require the detection of PERR#, set DevB:0x40[NMIONERR] to enable the generation of an NMI when DevA:0x1C[MDPE] is set.

Fix Planned
No

52 Some PCI Prefetching Control Settings Cause PCI Bus Performance to Degrade

Description
For certain PCI prefetching control settings in DevB:0x50 and DevB:0x54, the bus performance of the secondary PCI bus of the AMD-8111 HyperTransport I/O hub may be degraded.

Potential Effect on System
The data bandwidth of the secondary PCI bus may be degraded.

Suggested Workaround
BIOS programs the PCI prefetching mode in DevB:0x50 and DevB:0x54 according to the following table.

Register	Value
DevB:0x50	0000_0000h
DevB:0x54	0000_718Dh

Fix Planned
No

53 VDD_RTC Current in G3 May Exceed 8 μA Maximum

Description
The current on VDD_RTC in the G3 state can exceed the specified value of 8 μA, depending on the external crystal and the capacitors tied to VSS.

Potential Effect on System
None.

Suggested Workaround
None.

Fix Planned
No

54 USB in Reset Following Exit from S3 State

Description
The USB interface is in reset during resume from S3.

Potential Effect on System
None. Some operating systems may require not to reset the USB bus resuming from S3.

Suggested Workaround
None.

Fix Planned
No

55 Non-Posted Starvation Scenario with IDE or EHCI Controller

Description
If there is a continuous stream of downstream posted write transactions targeting the PCI bus at the same time as a non-posted (e.g., read) transaction targeting either the IDE controller or the EHCI controller, then the non-posted transaction may not complete until there is a gap in the stream of posted writes.

Potential Effect on System
A non-posted transaction may require an unusually long time to complete.

Suggested Workaround
None.

Fix Planned
No

56 DevB:3x64[5] Always Returns 0

Description
Read accesses to DevB:3x64[5] always returns 0 even if this bit is set.

Potential Effect on System
None.

Suggested Workaround
None.

Fix Planned
No

57 PCI Input Hold Time Violation

Description
The PCI input hold time specification is 0 ns. The AMD-8111 HyperTransport I/O hub input hold time requirement is 1.85 ns.

Potential Effect on System
Transfer of erroneous data and system deadlock is possible.

Suggested Workaround
None required. No failures related to this issue have been observed.

Fix Planned
No

58 Subtractive Decode Routing to the PCI Bus Not Supported

Description
The AMD-8111 I/O hub does not function properly when DevB:0x40[SUBDEC] is set. This bit is normally not set. When it is set, all unmapped host requests are routed to the PCI bus; if they are not claimed by the PCI bus, then they are routed to the LPC bus.

Potential Effect on System
Read or write data to the LPC bus may be corrupted.

Suggested Workaround
Leave DevB:0x40[SUBDEC] in the clear state.

Fix Planned
No

59 LPC Input Hold Time Violation

Description
The LPC input hold time specification is 0 ns. The AMD-8111 I/O hub input hold time requirement is 1.85 ns.

Potential Effect on System
Transfer of erroneous data and system deadlock is possible.

Suggested Workaround
None required. No failures related to this issue have been observed.

Fix Planned
No

60 CMOS Lock Control

Description
DevB:0x47[CMLK_B8 and CMLK_38] are specified to control read and write access to CMOS RAM locations B8-BF and 38-3F respectively. When a bit is clear, read and write access to the 8-byte range is allowed. When a bit is set, writes are disallowed and reads return FF's.

The AMD-8111 I/O hub returns FF's when reading from locked addresses but fails to block writes.

Potential Effect on System
None expected.

Suggested Workaround
None. There are no known useful purposes for this feature.

Fix Planned
No

61 I/O and LPC DMA Conflict

Description
The AMD-8111 HyperTransport I/O hub may corrupt I/O read or write data and DMA read data under the following conditions:

- A DMA read operation on the LPC bus is in progress.
- A read or write operation occurs to any of the I/O addresses 0x0022, 0x0023, 0x00A2, 0x00A3, 0x00F2, 0x00F3, 0x04D2, 0x04D3.

Potential Effect on System
Transfer of erroneous data and system deadlock is possible.

Suggested Workaround
Do not access the I/O addresses 0x0022, 0x0023, 0x00A2, 0x00A3, 0x00F2, 0x00F3, 0x04D2, or 0x04D3. In standard systems these addresses are not used for normal operation.

Fix Planned
No

62 Downstream Posted Write Completion Dependency On Upstream Posted Write Completion

Description
Under highly specific conditions, the AMD-8111 HyperTransport™ I/O hub Southbridge can fail to complete a downstream posted write.

Potential Effect on System
System hangs and/or a PCI bus lockup can occur.

Suggested Workaround
Map the address spaces behind the AMD-8111 to non-posted addresses. This is accomplished via the processor memory-mapped I/O limit registers (function 1: offsets 84h, 8Ch, 94h, 9Ch, A4h, ACh, B4h, and BCh). Each register contains an NP attribute bit (bit 7) which when set will cause all writes from the host bridge to be issued as non-posted. Set the NP attribute bit for the registers which correspond to the AMD-8111 address space. The same mapping to non-posted space will occur if any address ranges for the AMD-8111 are not included in any of these memory-mapped I/O registers. In this case, the addresses will be mapped as compat space and will be treated as non-posted.

Fix Planned
No

63 AMD-8111™ HyperTransport™ I/O Hub Lacks Extended Configuration Space Memory-Mapped I/O Base Address Register

Description
Current AMD processors do not natively support PCI-defined extended configuration space. A memory mapped I/O base address register (MMIO BAR) is required in chipset devices to support extended configuration space. The AMD-8111 does not have this MMIO BAR.

Potential Effect on System
The AMD-8111 is not a PCI-X® Mode 2 or PCI Express® capable device and is not required to support the MMIO BAR. However, using a device with an MMIO BAR and an AMD-8111 on the same HyperTransport™ link of the processor may cause firmware/software problems.

Suggested Workaround
It is strongly recommended that system designers do not connect the AMD-8111 and devices that use extended configuration space MMIO BARs (ex: HyperTransport-to-PCI Express bridges) to the same processor HyperTransport link.

Fix Planned
No

Documentation Support

The following documents provide additional information regarding the operation of the AMD-8111 HyperTransport I/O hub:

- *AMD-8111™ HyperTransport™ I/O Hub Data Sheet*, order# 24674
- *AMD-8111™ HyperTransport™ I/O Hub Design Guide*, order# 25517
- *BIOS and Kernel Developer's Guide for AMD Athlon™ 64 and AMD Opteron™ Processors*, order# 26094
- *HyperTransport™ I/O Link Specification*, revision 2.00a

See the AMD Web site at *www.amd.com* for the latest updates to documents. For documents subject to a Non-Disclosure Agreement (NDA), please contact your local sales representative.