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Revision Guide for AMD Family 17h Models 00h-0Fh Processors

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Advanced Micro Devices

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Revision History

Date	Revision	Description
May 2019	1.16	Added 2nd Generation AMD Ryzen™ Threadripper™ silicon information to Overview, Table 4, and Table 10; Added errata #1100, #1102, #1110, #1124, #1125, #1126, #1128, #1130, #1142, #1146, #1154, #1155, #1158, #1160, and #1163; Modified erratum #1076.
June 2018	1.12	Initial public release.

Overview

The purpose of the *Revision Guide for AMD Family 17h Models 00h-0Fh* is to communicate updated product information to designers of computer systems and software developers. This revision guide includes information on the following products:

- AMD Ryzen™ Processor
- 2nd Generation AMD Ryzen™ Processor
- AMD EPYC™ Processor
- AMD Ryzen™ Threadripper™ Processor
- 2nd Generation AMD Ryzen™ Threadripper™ Processor

Feature support varies by brands and OPNs (Ordering Part Number). To determine the features supported by your processor, contact your customer representative.

This guide consists of these major sections:

- Processor Identification shows how to determine the processor revision and workaround requirements, and to construct, program, and display the processor name string.
- Product Errata provides a detailed description of product errata, including potential effects on system operation and suggested workarounds. An erratum is defined as a deviation from the product's specification, and as such may cause the behavior of the processor to deviate from the published specifications.
- Documentation Support provides a listing of available technical support resources.

Revision Guide Policy

Occasionally, AMD identifies product errata that cause the processor to deviate from published specifications. Descriptions of identified product errata are designed to assist system and software designers in using the processors described in this revision guide. This revision guide may be updated periodically.

Conventions

Numbering

- **Binary numbers**. Binary numbers are indicated by appending a "b" at the end, e.g., 0110b.
- **Decimal numbers**. Unless specified otherwise, all numbers are decimal. This rule does not apply to the register mnemonics.
- **Hexadecimal numbers**. Hexadecimal numbers are indicated by appending an "h" to the end, e.g., 45F8h.
- **Underscores in numbers**. Underscores are used to break up numbers to make them more readable. They do not imply any operation. e.g., 0110_1100b.
- **Undefined digit**. An undefined digit, in any radix, is notated as a lower case "x".

Arithmetic and Logical Operators

In this document, formulas follow some Verilog conventions as shown in Table 1.

Table 1. Arithmetic and Logic Operators

Operator	Definition
{}	Curly brackets are used to indicate a group of bits that are concatenated together. Each set of bits is separated by a comma. E.g., {Addr[3:2], Xlate[3:0]} represents a 6-bit value; the two MSBs are Addr[3:2] and the four LSBs are Xlate[3:0].
|	Bitwise OR operator. E.g. (01b | 10b == 11b).
||	Logical OR operator. E.g. (01b || 10b == 1b); logical treats multibit operand as 1 if >=1 and produces a 1-bit result.
&	Bitwise AND operator. E.g. (01b & 10b == 00b).
&&	Logical AND operator. E.g. (01b && 10b == 1b); logical treats multibit operand as 1 if >=1 and produces a 1-bit result.
^	Bitwise exclusive-OR operator; sometimes used as "raised to the power of" as well, as indicated by the context in which it is used. E.g. (01b ^ 10b == 11b). E.g. (2^2 == 4).
~	Bitwise NOT operator (also known as one's complement). E.g. (~10b == 01b).
!	Logical NOT operator. E.g. (!10b == 0b); logical treats multibit operand as 1 if >=1 and produces a 1-bit result.
==	Logical "is equal to" operator.
!=	Logical "is not equal to" operator.
<=	Less than or equal operator.
>=	Greater than or equal operator.
*	Arithmetic multiplication operator.
/	Arithmetic division operator.
<<	Shift left first operand by the number of bits specified by the 2nd operand. E.g. (01b << 01b == 10b).
>>	Shift right first operand by the number of bits specified by the 2nd operand. E.g. (10b >> 01b == 01b).

Register References and Mnemonics

In order to define errata workarounds it is sometimes necessary to reference processor registers. References to registers in this document use a mnemonic notation consistent with that defined in the *Processor Programming Reference (PPR) for AMD Family 17 Model 00h-0Fh Processors*, order# 54945, or the *Open-Source Register Reference for AMD Family 17h Processors*, order# 56255.

Processor Identification

This section shows how to determine the processor revision.

Revision Determination

A processor revision is identified using a unique value that is returned in the EAX register after executing the CPUID instruction function 0000_0001h (CPUID Fn0000_0001_EAX).

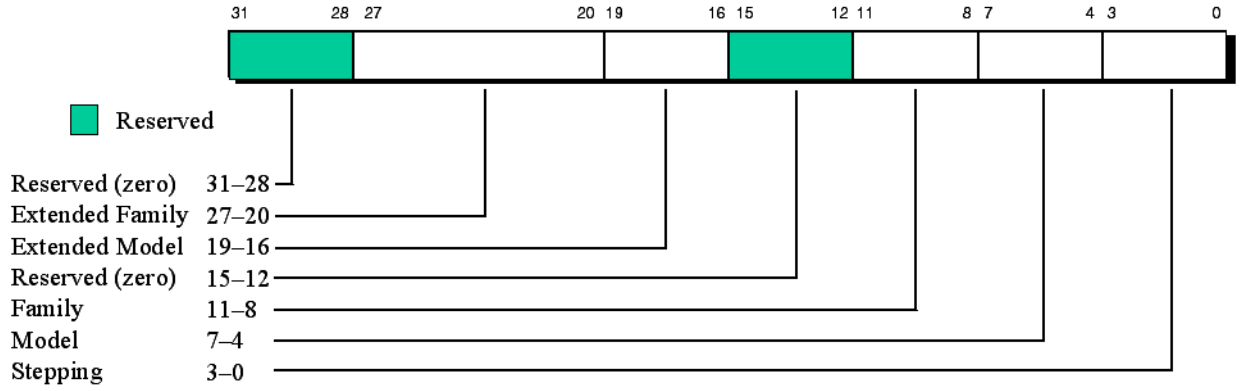

Figure 1. Format of CPUID Fn0000_0001_EAX

The following tables show the identification numbers from CPUID Fn0000_0001_EAX for each revision of the processor to each processor segment. "X" signifies that the revision has been used in the processor segment. "N/A" signifies that the revision has not been used in the processor segment.

Table 2. CPUID Values for AMD Family 17h Models 00h-0Fh SP3 Processor Revisions

CPUID Fn0000_0001_EAX (Mnemonic)	AMD EPYC™ Processors
00800F12h (ZP-B2)	X

Table 3. CPUID Values for AMD Family 17h Models 00h-0Fh AM4 Processor Revisions

CPUID Fn0000_0001_EAX (Mnemonic)	AMD Ryzen™ Processors	2nd Generation AMD Ryzen™ Processors
00800F11h (ZP-B1)	X	N/A
00800F82h (PiR-B2)	N/A	X

Table 4. CPUID Values for AMD Family 17h Models 00h-0Fh SP3r2 Processor Revisions

CPUID Fn0000_0001_EAX (Mnemonic)	AMD Ryzen™ Threadripper Processors	2nd Generation AMD Ryzen™ Threadripper Processors
00800F11h (ZP-B1)	X	N/A
00800F12h (ZP-B2)	N/A	X

Mixed Processor Revision Support

AMD Family 17h processors with different revisions may not be mixed in a multiprocessor system.

Programming and Displaying the Processor Name String

This section, intended for system software programmers, describes how to program and display the 48-character processor name string that is returned by CPUID Fn8000_000[4:2]. The hardware or cold reset value of the processor name string is 48 ASCII NUL characters, so system software must program the processor name string before any general purpose application or operating system software uses the extended functions that read the name string. It is common practice for system software to display the processor name string and model number whenever it displays processor information during boot up.

Note: *Motherboards that do not program the proper processor name string and model number will not pass AMD validation and will not be posted on the AMD Recommended Motherboard Web site.*

The name string must be ASCII NUL terminated and the 48-character maximum includes that NUL character.

The processor name string is programmed by MSR writes to the six MSR addresses covered by the range MSRC001_00[35:30]h. Refer to the PPR for the format of how the 48-character processor name string maps to the 48 bytes contained in the six 64-bit registers of MSRC001_00[35:30].

The processor name string is read by CPUID reads to a range of CPUID functions covered by CPUID Fn8000_000[4:2]. Refer to CPUID Fn8000_000[4:2] in the PPR for the 48-character processor name string mapping to the 48 bytes contained in the twelve 32-bit registers of CPUID Fn8000_000[4:2].

Operating System Visible Workarounds

This section describes how to identify operating system visible workarounds.

MSRC001_0140 OS Visible Work-around MSR0 (OSVW_ID_Length)

This register, as defined in *AMD64 Architecture Programmer's Manual Volume 2: System Programming*, order# 24593, is used to specify the number of valid status bits within the OS Visible Work-around status registers.

The reset default value of this register is 0000_0000_0000_0000h.

System software shall program the OSVW_ID_Length to 0005h prior to hand-off to the OS.

Table 5. OSVW ID Length Register

Bits	Description
63:16	Reserved.
15:0	**OSVW_ID_Length: OS visible work-around ID length**. Read-write.

MSRC001_0141 OS Visible Work-around MSR1 (OSVW_Status)

This register, as defined in *AMD64 Architecture Programmer's Manual Volume 2: System Programming*, order# 24593, provides the status of the known OS visible errata. Known errata are assigned an OSVW_ID corresponding to the bit position within the valid status field.

Operating system software should use MSRC001_0140 to determine the valid length of the bit status field. For all valid status bits: 1=Hardware contains the erratum, and an OS software work-around is required or may be applied instead of a system software workaround. 0=Hardware has corrected the erratum, so an OS software work-around is not necessary.

The reset default value of this register is 0000_0000_0000_0000h.

Table 6. OSVW Status Register

Bits	Description
63:5	**OsvwStatusBits:** Reserved. OS visible work-around status bits. Read-write.
4	**OsvwId4:** Reserved, must be zero.
3	**OsvwId3:** Reserved, must be zero.
2	**OsvwId2:** Reserved, must be zero.
1	**OsvwId1:** Reserved, must be zero.
0	**OsvwId0:** Reserved, must be zero.

System software shall program the state of the valid status bits as shown in Table 7 prior to hand-off to the OS.

Table 7. Cross Reference of Product Revision to OSVW ID

CPUID Fn0000_0001_EAX (Mnemonic)	MSRC001_0141 Bits
00800F11h (ZP-B1)	0000_0000_0000_0000h

Table 7. Cross Reference of Product Revision to OSVW ID (continued)

CPUID Fn0000_0001_EAX (Mnemonic)	MSRC001_0141 Bits
00800F12h (ZP-B2)	0000_0000_0000_0000h
00800F82h (PiR-B2)	0000_0000_0000_0000h

Product Errata

This section documents product errata for the processors. A unique tracking number for each erratum has been assigned within this document for user convenience in tracking the errata within specific revision levels. This table cross-references the revisions of the part to each erratum. "No fix planned" indicates that no fix is planned for current or future revisions of the processor.

Note: There may be missing errata numbers. Errata that do not affect this product family do not appear. In addition, errata that have been resolved from early revisions of the processor have been deleted, and errata that have been reconsidered may have been deleted or renumbered.

Table 8. Cross-Reference of Processor Revision to Errata

No.	Errata Description	CPUID Fn0000_0001_EAX		
		00800F82h (PiR-B2)	00800F11h (ZP-B1)	00800F12h (ZP-B2)
911	IOMMU Unnecessarily Updates Dirty Bit (D-bit) While Handling Non-supervisor DMA Write Request To Writable Supervisor-only Page	No fix planned		
913	IOMMU Incorrectly Issues Guest Page Table Walk Request as Non-coherent Request	No fix planned		
919	USB tPortConfiguration Timer Incorrectly Resets During Recovery Before LMP (Link Management Packet) Exchange	No fix planned		
923	IOMMU Event Not Logged When Software Programs DTE.HAD Bits Incorrectly	No fix planned		
931	MCA_MISC0[BlkPtr] May Contain Incorrect Value	No fix planned		
937	Unpredictable IOMMU IO_PAGE_FAULT Event Logging For PCIe® Atomic Requests To Protected Pages	No fix planned		
954	Processor Will Shut Down If It Issues a Load That Consumes Poison Data When Error Reporting is Disabled	No fix planned		
955	Processor May Stall If Error Reporting is Disabled and a Cacheable Lock or Table-Walk Load Encounters a Master Abort, Target Abort, or Protection Violation	No fix planned		
965	Incorrect IOMMU IO_PAGE_FAULT Event Logging For Reserved Message Type Interrupt Requests With DTE.IG = 1	No fix planned		
990	Certain Performance Counters For Retire Based Events May Overcount	No fix planned		
1017	FERR (Legacy Floating Point Error) for Thread 0 May be Incorrectly Cleared When Thread 1 Clears Its FERR		X	
1021	Load Operation May Receive Stale Data From Older Store Operation	No fix planned		
1023	Performance Monitor Counter Overflow Interrupts May Fail To Be Delivered When Two or More Counters Are Enabled		X	
1024	Cacheable Load Following Misaligned Cacheable Store Does Not Complete	No fix planned		
1033	A Lock Operation May Cause the System to Hang		X	
1034	Processor May Return Incorrect Faulting Linear Address For a Cacheline-Misaligned Store		X	
1036	When IOMMU Interrupt Remapping Is Enabled the Remapped TM (Trigger Mode) Bit Is Incorrectly Ignored		X	
1037	USB 2.0 Device May Immediately Reconnect After Windows® "Safely Remove Hardware" Procedure	No fix planned		
1038	xHCI Controller May Incorrectly Drop USB 3.0 ISOC Audio Packets		X	
1039	Non-Cacheable Coherent Store May Not Complete If it Follows a Cacheable Access to the Same Cache Line		X	
1042	Processor May Fail To Boot On Systems With Both SPI (Serial Peripheral Interface) and Discrete TPM (Trusted Platform Module) Enabled	No fix planned		
1043	IOMMU May Fail to Deliver an Interrupt or Incorrectly Send an Interrupt to the Host OS	No fix planned		
1044	PCIe® Controller May Hang on Entry Into Either L1.1 or L1.2 Power Management Substate		X	

Table 8. Cross-Reference of Processor Revision to Errata (continued)

No.	Errata Description	CPUID Fn0000_0001_EAX		
		00800F82h (PiR-B2)	00800F11h (ZP-B1)	00800F12h (ZP-B2)
1047	Miss Address Buffer Performance Counter May Be Inaccurate	No fix planned		
1048	Three-Source Operand Floating Point Instructions May Block Another Thread on the Same Core	No fix planned		
1049	FCMOV Instruction May Not Execute Correctly	No fix planned		
1053	When SMAP is Enabled and EFLAGS.AC is Set, the Processor Will Fail to Page Fault on an Implicit Supervisor Access to a User Page	No fix planned		
1054	Instructions Retired Performance Counter May Be Inaccurate	No fix planned		
1057	MWAIT or MWAITX Instructions May Fail to Correctly Exit From the Monitor Event Pending State		X	X
1058	Executing Code in the Page Adjacent to a Canonical Address Boundary May Cause Unpredictable Results	No fix planned		
1059	In Real Mode or Virtual-8086 Mode MWAIT or MWAITX Instructions May Fail to Correctly Exit From the Monitor Event Pending State	No fix planned		
1063	PCIe® Controller Will Generate MSI (Message Signaled Interrupt) With Incorrect Requestor ID	No fix planned		
1067	L3 Performance Event Counter May Be Inaccurate	No fix planned		
1070	16-bit Real Mode Applications May Fail When Virtual Mode Extensions (VME) Are Enabled	No fix planned		
1071	Spurious Level 2 Branch Target Buffer (L2 BTB) Multi-Match Error May Occur	No fix planned		
1076	CPUID Fn8000_0007_EDX[CPB] Incorrectly Returns 0		X	
1080	PCIe® Link Exit to L0 in Gen1 Mode May Incorrectly Trigger NAKs		X	X
1081	Programming MSRC001_0015 [Hardware Configuration] (HWCR)[CpbDis] Does Not Affect All Threads In The Socket		X	X
1083	PCIe® Link in Gen3 Mode May Incorrectly Observe EDB Error and Enter Recovery		X	X
1084	xHCI Host May Fail To Respond to Resume Request From Downstream USB Device Within 1 ms	No fix planned		
1091	4K Address Boundary Crossing Load Operation May Receive Stale Data	No fix planned		
1092	USB Device May Not be Enumerated After Device Reset	No fix planned		
1095	Potential Violation of Read Ordering In Lock Operation In SMT (Simultaneous Multithreading) Mode	No fix planned		
1096	The GuestInstrBytes Field of the VMCB on a VMEXIT May Incorrectly Return 0h	No fix planned		
1100	A Page Fault on a User Mode Fused Branch Instruction May Stall	No fix planned		
1102	The Processor May Hang During Warm Reset	No fix planned		
1108	MCA Error May Incorrectly Report Overflow Condition	No fix planned		
1109	MWAIT Instruction May Hang a Thread		X	X
1110	Inaccurate Deferred Errors May Be Logged in MCA_STATUS_CS After Warm Reset	No fix planned		
1124	A Short Circuit Event on Any USB Port Will Cause xHCI/EHCI Controller Failure	No fix planned		
1125	Reading or Writing Certain PCIe® Registers in a PCIe Root Port May Cause the Processor to Hang		X	X
1126	PCIe® Link May Hang When Attempting to Switch to Gen3 Mode	No fix planned		
1128	Incorrect Error Codes For Benign VMM Communication (#VC) Exceptions			X
1130	Certain Sequences of Instructions May Cause Incorrect Memory Reference Address	No fix planned		
1142	Locked Operations Involving Page Table Entries May Observe Stale Accessed Bit	No fix planned		

Table 8. Cross-Reference of Processor Revision to Errata (continued)

No.	Errata Description	CPUID Fn0000_0001_EAX		
		00800F82h (PiR-B2)	00800F11h (ZP-B1)	00800F12h (ZP-B2)
1146	PCIe® DPC (Downstream Port Containment) RP PIO (Root Port Programmed I/O) Error Reporting May Not Function Correctly	No fix planned		
1154	MOV SS Instructions May Take Multiple Breakpoints	No fix planned		
1155	DMA or Peer-to-peer Accesses Using Guest Physical Addresses (GPAs) May Cause IOMMU Target Abort	No fix planned		
1158	Local Interrupts LINT0/LINT1 May Occur While APIC is Software Disabled	No fix planned		
1160	SdpParity and XiVictimQueue Mask Bits Incorrectly Mask Additional Errors	No fix planned		
1163	Some MCA_MISC0 Bits May Fail to Persist Through Warm Reset	No fix planned		