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## Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>March 2006</td>
<td>3.06</td>
<td>Added erratum #28.</td>
</tr>
<tr>
<td>August 2004</td>
<td>3.04</td>
<td>Added erratum #27.</td>
</tr>
<tr>
<td>June 2003</td>
<td>3.00</td>
<td>Initial public release.</td>
</tr>
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The purpose of the AMD-8151™ HyperTransport™ AGP3.0 Graphics Tunnel Revision Guide is to communicate updated product information on the AMD-8151™ HyperTransport™ AGP3.0 graphics tunnel to designers of computer systems and software developers. This guide consists of three major sections:

- **Revision Determination**: This section, which starts on page 6, describes the mechanism by which the current revision of the part is identified.

- **Product Errata**: This section, which starts on page 7, provides a detailed description of product errata, including potential effects on system operation and suggested workarounds. An erratum is defined as a deviation from product specifications, and as such may cause the behavior of the AMD-8151 HyperTransport AGP3.0 graphics tunnel to deviate from the published specifications.

- **Documentation Support**: This section, which starts on page 15, provides a listing of available technical support resources.

**Revision Guide Policy**

Occasionally, AMD identifies product errata that cause the AMD-8151 HyperTransport AGP3.0 graphics tunnel to deviate from published specifications. Descriptions of identified product errata are designed to assist system and software designers in using the AMD-8151 HyperTransport AGP3.0 graphics tunnel. Furthermore, this revision guide may be updated periodically.
Revision Determination

The BIOS checks the PCI revision ID register at DevA:0x08 to determine the version of silicon as shown in Table 1.

Table 1. AMD-8151™ HyperTransport™ AGP3.0 Graphics Tunnel Revision IDs

<table>
<thead>
<tr>
<th>Sequence</th>
<th>Revision</th>
<th>DevA:0x08</th>
<th>DevB:0x08</th>
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<tbody>
<tr>
<td>5</td>
<td>B2</td>
<td>13h</td>
<td></td>
</tr>
</tbody>
</table>
Product Errata

This section documents AMD-8151™ HyperTransport™ AGP3.0 graphics tunnel product errata. A unique tracking number for each erratum has been assigned within this document for user convenience in tracking the errata within specific revision levels. Table 2 cross-references the revisions of the part to each erratum. An “X” indicates that the erratum applies to the revision. The absence of an “X” indicates that the erratum does not apply to the revision.

Note: There may be missing errata numbers. Errata that have been resolved from early revisions of the device have been deleted, and errata that have been reconsidered may have been deleted or renumbered.

<table>
<thead>
<tr>
<th>Errata Numbers and Description</th>
<th>Revision Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>22 Incorrect Value For DevA:0xA4[Host translation#]</td>
<td>X</td>
</tr>
<tr>
<td>23 Link Electrical Issue When Operating At 800 MHz</td>
<td>X</td>
</tr>
<tr>
<td>24 Deadlock Scenario With Peer-To-Peer Traffic</td>
<td>X</td>
</tr>
<tr>
<td>25 Input Leakage Parameter Out Of Spec</td>
<td>X</td>
</tr>
<tr>
<td>26 DevB:0x00[DevID] Is Read Only</td>
<td>X</td>
</tr>
<tr>
<td>27 Failure When B-Side Link Is Directed Toward The Host</td>
<td>X</td>
</tr>
<tr>
<td>28 The AMD-8151™ Tunnel Lacks Extended Configuration Space Memory-Mapped I/ O Base Address Register</td>
<td>X</td>
</tr>
</tbody>
</table>
22 Incorrect Value For DevA:0xA4[Host translation#]

Description
DevA:0xA4[Host translation#] is a read-only bit, fixed in the high state in the graphics tunnel. Per the AGP specification, this indicates that core logic does not translate host transactions addressed to the Graphics Aperature through the GART. However, on AMD platforms that use the graphics tunnel, such host transactions can be translated through the GART.

Potential Effect on System
None.

Suggested Workaround
Software should presume that this bit is low for the graphics tunnel.

Fix Planned
Yes
23 Link Electrical Issue When Operating At 800 MHz

Description
The graphics tunnel A-side link may not operate properly at 800 MHz.

Potential Effect on System
Transfer of erroneous data and system deadlocks are possible.

Suggested Workaround
The A-side link should be configured to operate at 600 MHz instead of 800 MHz.
Alternatively, more restrictive system board layout rules for the A-side link may be employed. See the AMD-8151 HyperTransport AGP3.0 Graphics Tunnel Motherboard Design Guide, order# 25617 for details.

Fix Planned
No
24  Deadlock Scenario With Peer-To-Peer Traffic

Description

Some PCI cards generate peer-to-peer posted-write traffic targeting the AGP bridge (from the PCI bus, through the graphics tunnel, to the host, back to the graphics tunnel to the AGP bus). The combination of such cards and some AGP cards can generate traffic patterns that result in a system deadlock.

Potential Effect on System

The system deadlocks.

Suggested Workaround

Do not support PCI cards that generate peer-to-peer traffic to the AGP bridge.

Fix Planned

Yes
25  Input Leakage Parameter Out Of Spec

Description

When operating with AGP2.0 signaling, the input leakage current ($I_{IL}$) is specified to be limited to less than ±10 $\mu$A. However, input leakage current may be as much as ±20 $\mu$A in some graphics tunnel parts.

Potential Effect on System

None.

Suggested Workaround

None required.

Fix Planned

No
26  DevB:0x00[DevID] Is Read Only

Description
The four LSBs of DevB:0x00[DevID] should be "write once". However, they are "read only" instead.

Potential Effect on System
A generic graphics driver may be loaded even if the platform does not support the generic driver.

Suggested Workaround
None required.

Fix Planned
Yes
27 Failure When B-Side Link Is Directed Toward The Host

Description
The AMD-8151 does not master abort a transaction with the HyperTransport COMPAT bit set if all of the following conditions apply:

- HyperTransport link B is connected toward the host
- HyperTransport link A is the end of chain

Potential Effect on System
The processor will hang.

Suggested Workaround
Connect the AMD-8151 HyperTransport interface A toward the processor.

Fix Planned
No
28 The AMD-8151™ Tunnel Lacks Extended Configuration Space Memory-Mapped I/O Base Address Register

Description

Current AMD processors do not natively support PCI-defined extended configuration space. A memory-mapped I/O base address register (MMIO BAR) is required in chipset devices to support extended configuration space. The AMD-8151 does not have this MMIO BAR.

Potential Effect on System

The AMD-8151 is not a PCI-X® Mode 2 or PCI Express® capable device and is not required to support the MMIO BAR. However, using a device with an MMIO BAR and an AMD-8151 on the same HyperTransport™ link of the processor may cause firmware/software problems.

Suggested Workaround

It is strongly recommended that system designers do not connect the AMD-8151 and devices that use extended configuration space MMIO BARs (ex: HyperTransport-to-PCI Express bridges) to the same processor HyperTransport link.

Fix Planned

No
The following documents provide additional information regarding the operation of the AMD-8151™ HyperTransport™ AGP3.0 graphics tunnel:

- **AMD-8151™ HyperTransport™ AGP3.0 Graphics Tunnel Data Sheet**, order# 24888
- **HyperTransport™ I/O Link Specification** (www.hypertransport.org)

See the AMD Web site at [www.amd.com](http://www.amd.com) for the latest updates to documents. For documents subject to a non-disclosure agreement, please contact your local sales representative.