AMD
Smarter Choice

GCC Quick Reference Guide

(versions 4.3.0 and later)

Aggressive GCC optimization flags:

-O3 -funroll-all-loops -ffast-math
-mtune=amdfam10 -fprefetch-loop-arrays -ftree-parallelize-loops=n

Flag	Purpose
-combine	Allows simultaneous optimization of multiple source files
-fprofile-generate -fprofile-use	Enables profile guided optimization; Particularly useful for cases that use data sets with similar characteristics (see man page for details)
-ffast-math	Accelerates mathematical operations (Note: Results may not be exact; Does not follow IEEE or ISO math specifications)
-fopenmp	OpenMP 2.5 / libgomp support (GCC 4.2.0 and later)
-fprefetch-loop-arrays	Generates instructions to prefetch memory to improve the performance of loops that access large arrays
-ftree-parallelize-loops=n	Enables auto parallelizing of loops
-funroll-all-loops	Minimizes loop overhead
-fwhole-program	Makes all global functions and variables static
-mtune=amdfam10	Optimizes for AMD Family 10h ("Barcelona") processors
-O3	Aggressive optimization (see man page for details), Previous auto-vectorization options such as -ftree-vectorize and -fvect-cost-model are now part of -O3 for GCC 4.3.0

Options for AMD "Barcelona" processors, such as AMD Phenom™ X4, AMD Phenom™ X3, and Quad-Core AMD Opteron™ processors, and for future AMD processors:

-mabm	Enable Advanced Bit Manipulation instructions lzcnt and popcnt
-msse4a	Enable SSE4a instruction set extensions
-march=amdfam10	Activates MMX, SSE, SSE2, SSE3, SSE4a, and ABM instructions and tunes for AMD Family 10h ("Barcelona") processors (Note: Provides superior performance to -mtune but may introduce instructions not supported on non-target platforms)
-msse5	Enables proposed SSE5 instruction set extensions (see AMD64 128-bit SSE5 Instruction Set (http://www.amd.com/us-en/assets/content_type/white_papers_and_techdocs/43479.pdf)

For more detailed information, go to:

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